Amendments to the Specification

Please amend the paragraph bridging pages 18 and 19 and the first full paragraph on page 19 as follows:

In mounting semiconductor devices on the surface of a BGA substrate, it is important from a manufacturing point of view that solder flux, after the process of solder flow has been completed, can be readily removed. This requires easy access to the surface areas of the BGA substrate where solder flux has been able to accumulate. In addition, the device interconnects (consisting of pillar metal and solder bumps) must, after the pillar metal and the solder bumps have been formed in accordance with the related application, be readily available so that device encapsulants can be adequately applied. More importantly, after flip-chip assembly and solder reflow, the flux that has accumulated in the gap between the semiconductor die and the substrate must be cleaned. For these reasons, it is of value to apply the solder mask not across the entire surface of the substrate (blank deposition) but to leave open the surface areas of the substrate that are immediately adjacent to the I/O interconnects (of pillar metal and solder bumps). This design will create a channel though which the cleaning solution can flow easily. This is highlighted in the top view of Figs. 11 and 12, where is shown:

- 52, the BGA substrate on the surface of which device 50 (not shown) is mounted
- 74, I/O contact pads provided on the surface of substrate 52
- 76, interconnect traces provided on the surface of substrate 52, connected with contact pads 74

- ~~78~~79, the surface region of the substrate 52 over which no solder mask is applied

- 80, the surface region of the substrate 52 over which a solder mask is applied.

This is further highlighted in the cross section of substrate 52 that is shown in Fig. 12. It is clear that over the region ~~78~~79, which is the region where no solder mask is applied, the metal pads 74 are readily available so that removal of solder flux and the dispensing of encapsulants can be performed. It must be remembered that this is possible due to the height of the combined pillar metal 54 and the solder bump 56, which results in adequate spacing between the device 50 and the surface of substrate 52. Further shown in Fig. 12 are routing traces 82 that are provided on the surface of substrate 52 for additional interconnect.